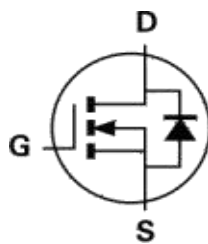


N-Channel Super Junction MOSFET 650V/20A

Parameter	Value	Unit
VDS	650	V
RDS(on)	165	mΩ
ID	20	A



TO-220F

FEATURES

- Ultra low RDS(on)
- Ultra low gate charge (typ. Qg=38.4nC)
- 100% UIS tested

APPLICATIONS

- Power factor correction (PFC)
- Switched mode power supplies (SMPS)
- Uninterruptible power supply (UPS)

MAXIMUM RATED VALUES

Parameter	Symbol	Value	Unit
Drain-Source Voltage	VDS	650	V
Gate-Source Voltage	VGS	±30	V
Continue Drain Current	ID	20	A
Pulsed Drain Current (Note1)	IDM	60	A
Power Dissipation	PD	34	W
Single Pulse Avalanche Energy (Note1)	EAS	600	mJ
Operating Temperature Range	TJ	-55 to +150	°C
Storage Temperature Range	TSTG	-55 to +150	°C
Thermal Resistance, Junction to Case	RθJC	3.7	°C/W
Thermal Resistance, Junction to Ambient	RθJA	62	°C/W

Note1:Pulse test: 300 μs pulse width, 2 % duty cycle

ELECTRICAL CHARACTERISTICS (at TJ = 25°C unless otherwise specified)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS = 0 V, ID = 250 μA	BVDSS	650	-	-	V

Drain-Source Leakage Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}	-	-	1	μA
Gate Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	$V_{GS(th)}$	2.5	-	4.5	V
Drain-Source On-State Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	$R_{DS(on)}$	-	165	180	m Ω
Forward Trans conductance	$V_{DS} = 40\text{ V}, I_D = 10\text{ A}$	g_{fs}	-	17	-	S
Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 100\text{ KHz}$	C_{iss}	-	1832	-	pF
Output Capacitance		C_{oss}	-	72.2	-	pF
Reverse Transfer Capacitance		C_{rss}	-	0.72	-	pF
Turn-on Delay Time(Note2)	$V_{DD} = 400\text{ V}$ $I_D = 10\text{ A}$ $V_{GS} = 10\text{ V}$ $R_G = 10\text{ }\Omega$	$t_d(ON)$	-	77	-	ns
Rise Time(Note2)		t_r	-	14.6	-	ns
Turn-Off Delay Time(Note2)		$t_d(OFF)$	-	64.4	-	ns
Fall Time(Note2)		t_f	-	6.2	-	ns
Total Gate Charge(Note2)	$V_{DS} = 520\text{ V}$ $V_{GS} = 10\text{ V}$ $I_D = 10\text{ A}$	Q_G	-	38.4	-	nC
Gate to Source Charge(Note2)		Q_{GS}	-	10.2	-	nC
Gate to Drain Charge(Note2)		Q_{GD}	-	14.6	-	nC

Source-Drain Diode Characteristics at $T_a = 25^\circ\text{C}$ unless otherwise specified

Parameter	Test Condition	Symbol	Min.	Typ.	Max.	Unit
Maximum Continuous Drain-Source Diode Forward Current		I_S	-	-	20	A
Maximum Pulsed Drain-Source Diode Forward Current		I_{SM}	-	-	60	A
Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}, T_J = 25^\circ\text{C}$	V_{SD}	-	-	1.1	V
Reverse recovery time	$T_J = 25^\circ\text{C}, I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	t_{rr}	-	302	-	ns
Reverse recovery charge		Q_{rr}		3616		nC

Note2: Pulse test: 300 μs pulse width, 2 % duty cycle

ELECTRICAL CHARACTERISTICS (at $T_J = 25^\circ\text{C}$ unless otherwise specif)

Fig 1: Output Characteristics

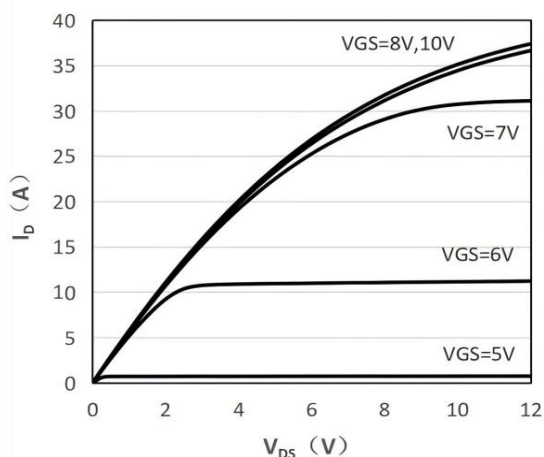


Fig 2: Transfer Characteristics

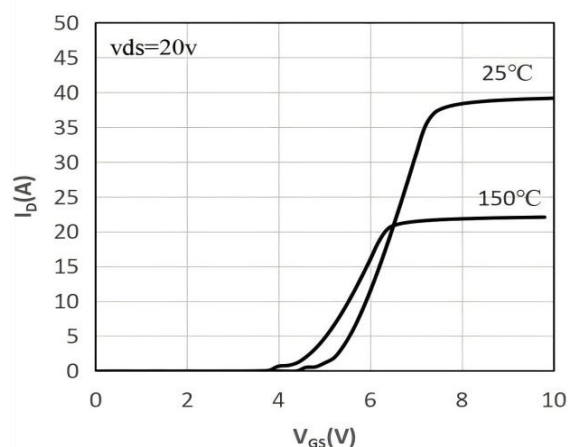


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

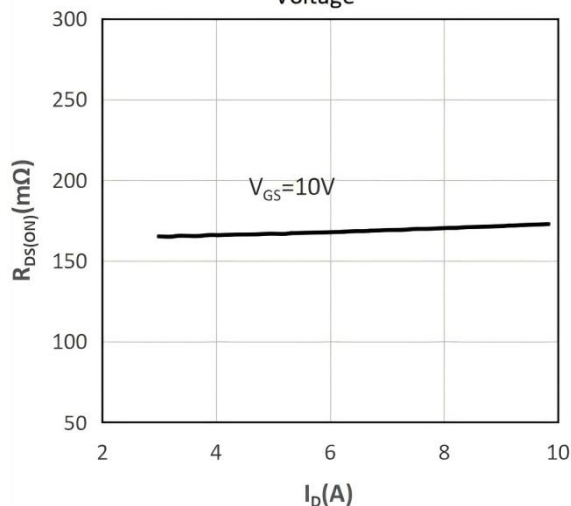


Fig 4: $R_{DS(on)}$ vs. Temperature

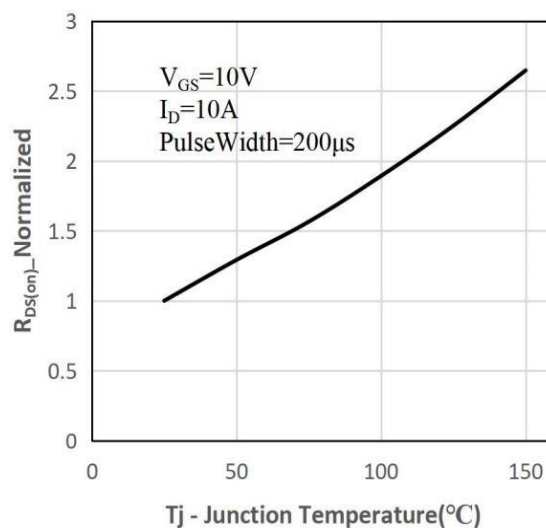


Fig 5: Breakdown Voltage vs. Temperature

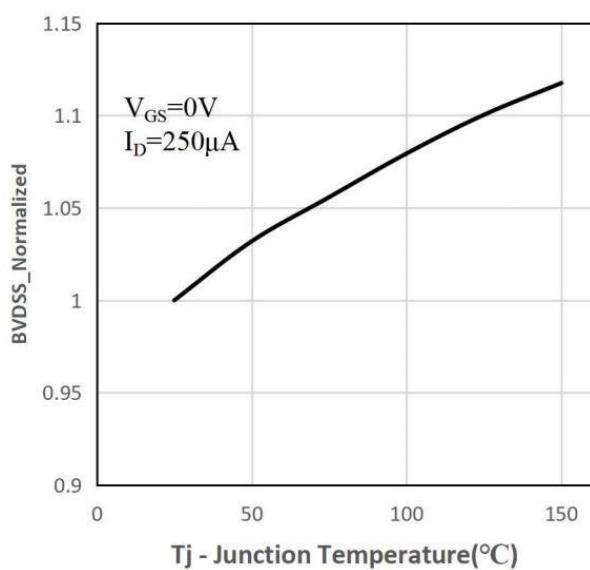


Fig 6: Threshold voltage vs. Temperature

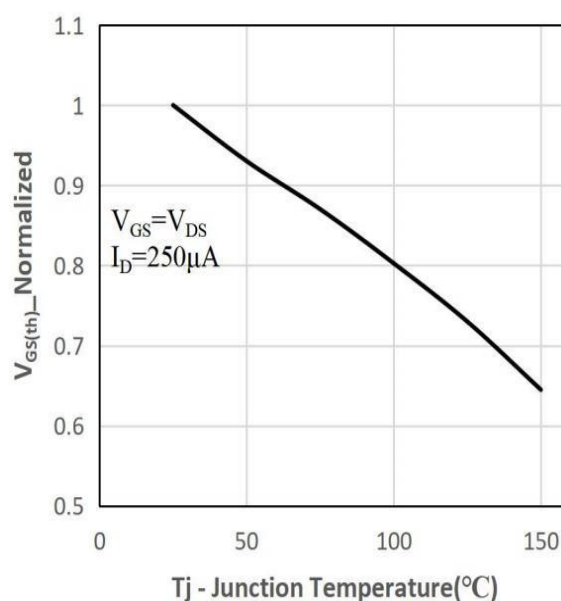


Fig 7: Body-Diode Characteristics

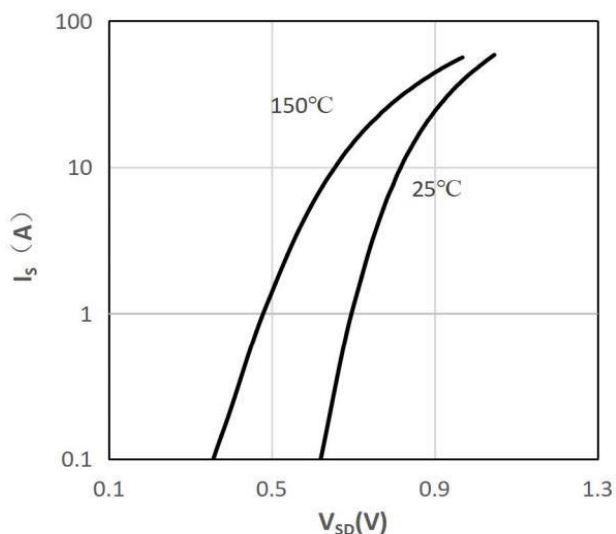


Fig 8: Capacitance Characteristics

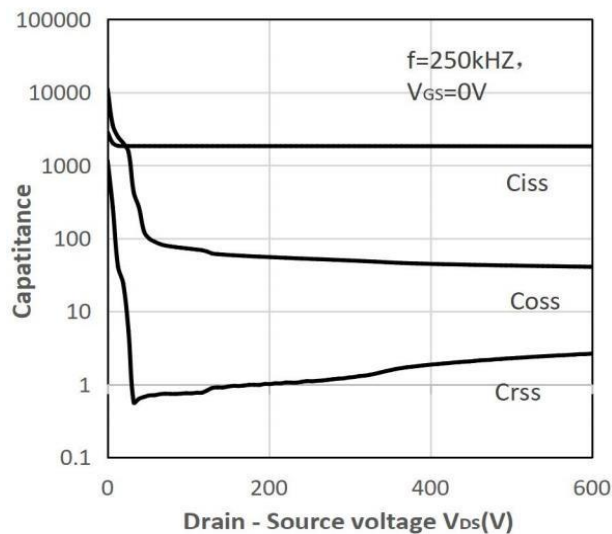


Fig 9: Gate Quantity of electric charge vs. Gate Voltage

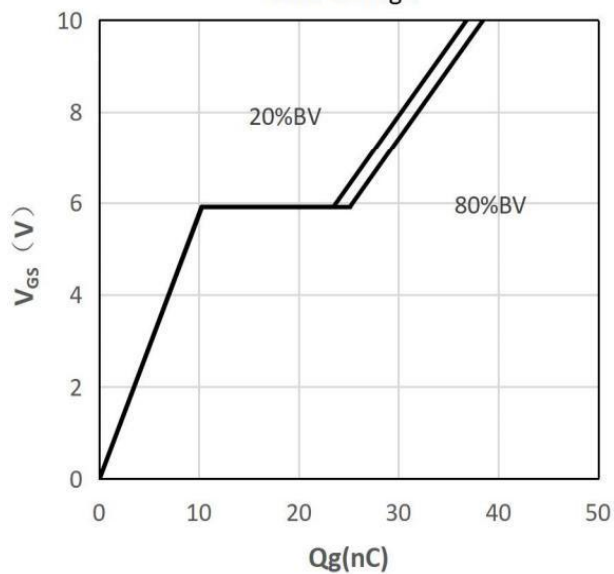


Fig 10: Drain Current Derating

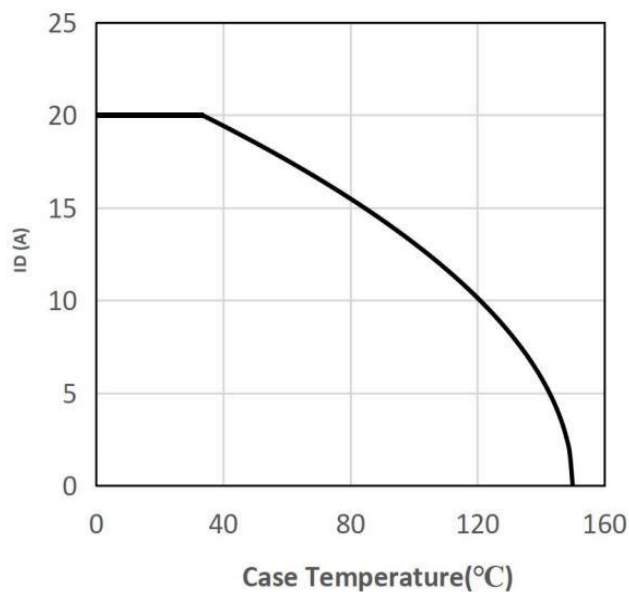


Fig 11: Power Dissipation vs. Temperature

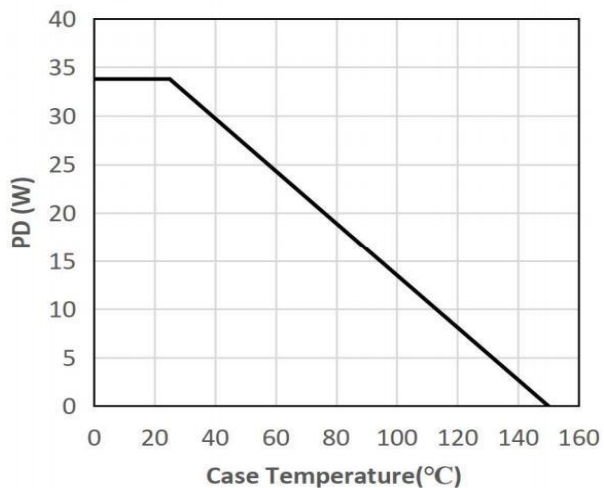
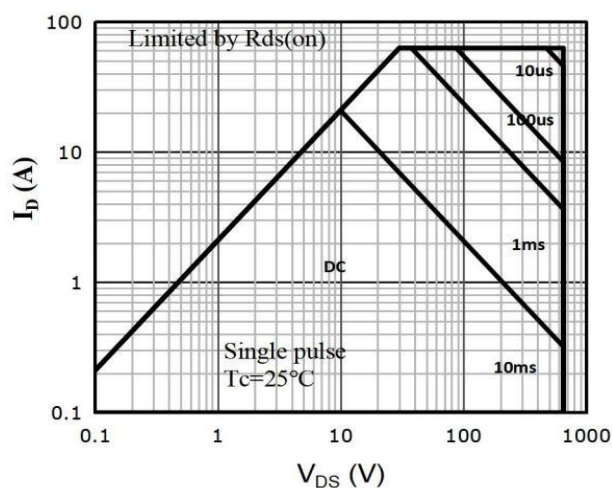
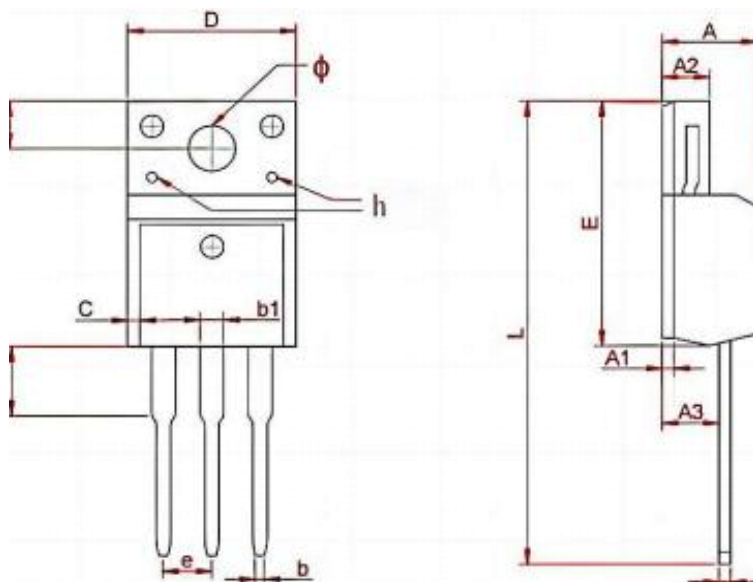


Fig 12: Safe Operating Area



PACKAGE OUTLINES



Symbol	Dimensions in mm	
	Min	Max
A	4.300	4.750
A1	0.7 REF	
A2	2.300	2.850
A3	2.500	2.900
b	0.380	0.420
b1	1.220	1.280
C	1.08	1.200
c	0.480	0.520
D	10.15	10.450
E	15.700	15.950
e	2.574 TYP	
F	3.470 REF	
y	3.200 REF	
h	0.000	0.800
L	28.780	28.900
L1	2.990	3.100

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- 1) Comply with applicable safety standards in designing a secure system architecture;
- 2) Implement redundancy, fire-prevention measures, and malfunction prevention protocols;
- 3) Mitigate risks of accidents, fires, or societal damages resulting from product use.
- 4) Designers must ensure Hypersemi products operate strictly within specified parameters defined in the latest product specifications.