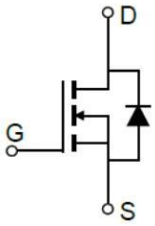
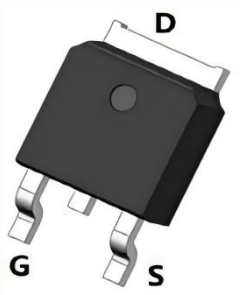
N-Channel Enhancement Mode MOSFET 30V/80A

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),typ}$	4.1	mΩ
I_D	80	A
$V_{GS(th).typ}$	1.5	V





TO-252

Features

- Si N-channel trench MOSFET
- Low gate charge
- Low Ciss
- Fast switching

Applications

- PWM applications
- Load switch
- Power management

MAXIMUM RATINGS (Ta=25°Cunless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current TA=25°C	I_D	80	A
Continuous Drain Current TA=100°C	I_D	50	A
Pulsed Drain Current	$I_{D.pulse}$	320	A
Maximum Power Dissipation Tc=25°C	P_D	70	W
Maximum Power Dissipation TA=25°C	P_D	2.8	W
Single Pulse Avalanche Energy (L=0.5mH, VD=24V, TC=25°C)	E_{AS}	110	mJ
Operating Junction Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTIC

Parameter		Symbol	Value	Unit
Thermal Resistance from Junction to Ambient(t≤10s)	PCB Mount	$R_{\theta JA}$	44	°CW
Thermal Resistance Junction-Case		$R_{\theta JC}$	1.95	°CW

ELECTRICAL CHARACTERISTICS(Ta=25°C unless otherwise noted)

Static Characteristics

Parameter	Symbol	Test condition	Values			Unit
			Min.	Typ.	Max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_C=250rA	30	-	-	V
Drain-source leakage current	I_{DSS}	V_{DS}=30V, V_{GS}=0V	-	-	1	uA
Gate leakage current, forward	I_{GSSF}	V_{GS}=20V, V_{DS}=0V	-	-	100	nA
Gate leakage current, reverse	IG_{SSR}	V_{GS}=-20V, V_{DS}=0V	-	-	-100	
Gate-source threshold voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250uA	1.0	1.5	2.0	V
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=15A	-	4.1	6	mΩ
		V_{GS}=4.5V, I_D=10A	-	7.0	10	
Forward Transconductance	gfs	V_{DS}=5V, I_D=20A	-	25	-	S

Note :

The data tested by surface mounted on a 1 inch2 FR-4 board with 2 oz copper.

The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%

The power dissipation is limited by 150℃ junction temperature

The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

Dynamic Characteristics

Parameter	Symbol	Test condition	Values			Unit
			Min.	Typ.	Max.	
Input capacitance	C_{iss}	V_{DS}=15V V_{GS}=0V f =1MHz	-	1558	-	pF
Output capacitance	C_{oss}		-	204	-	pF
Reverse transfer capacitance	C_{rss}		-	195	-	pF
Total gate charge	Q_g	V_{DS}=24V I_D=20A V_{GS}=10V	-	36	-	nC
Gate-source charge	Q_{gs}		-	7	-	nC
Gate-drain charge	Q_{gc}		-	9	-	nC
Gate resistance	R_g	V_{DS}=V_{GS}=0V, f =1MHz	-	5.8	-	Ω

Switching Characteristics

Parameter	Symbol	Test condition	Values			Unit
			Min.	Typ.	Max.	
Turn-on delay time	td(on)	VDD=15V VGS=10V ID=20A RG=10Ω	-	10	-	ns
Rise time	tr		-	45	-	ns
Turn-off delay time	td(off)		-	99	-	ns
Fall time	tf		-	55	-	ns

ELECTRICAL CHARACTERISTICS OF BODY DIODE (TJ=25oC unless otherwise noted)

Parameter	Symbol	Test condition	Values			Unit
			Min.	Typ.	Max.	
Body diode forward voltage	V_{SD}	I_{SD}=20A, V_{GS}=0V	-	-	1.2	V
Continuous diode forward current	I_{SD}	V_{GS}=0V	-	-	80	A
Pulsed diode current	I_{SM}	Pulse width≤380μs; duty cycle≤2%.	-	-	320	
Reverse recovery time	t_{rr}	V_{GS}=0V I_S= 15A di/dt=100A/rs	-	18	-	ns
Diode reverse recovery charge	Q_{rr}		-	10	-	nC

TYPICAL PERFORMANCE CHARACTERISTICS

Fig 1: Output Characteristics Tj=25℃

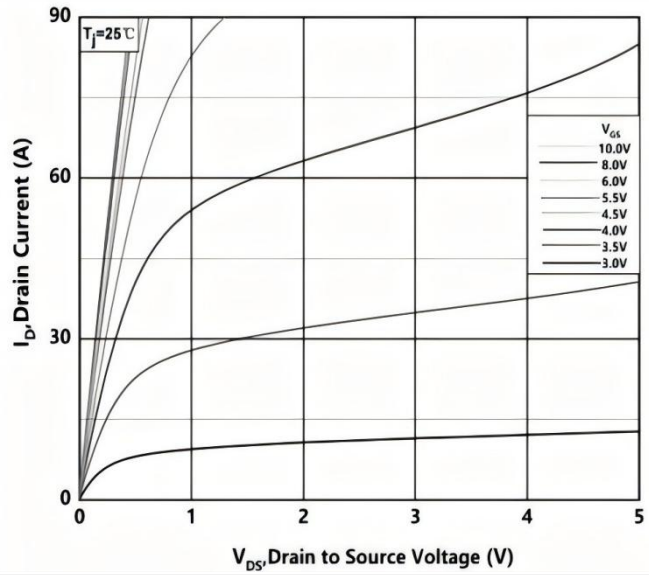


Fig 3: On-Resistance vs. Drain Current and Gate Voltage

Fig 2: Transfer Characteristic for Various Junction Temperatures

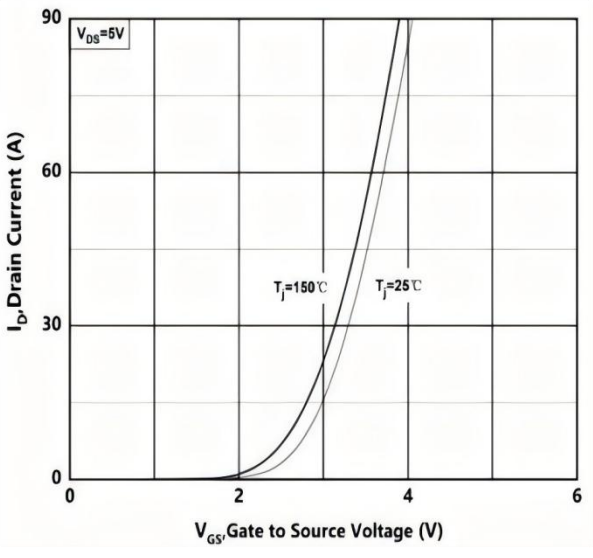


Fig 4: Typical On-Resistance vs Junction Temperature

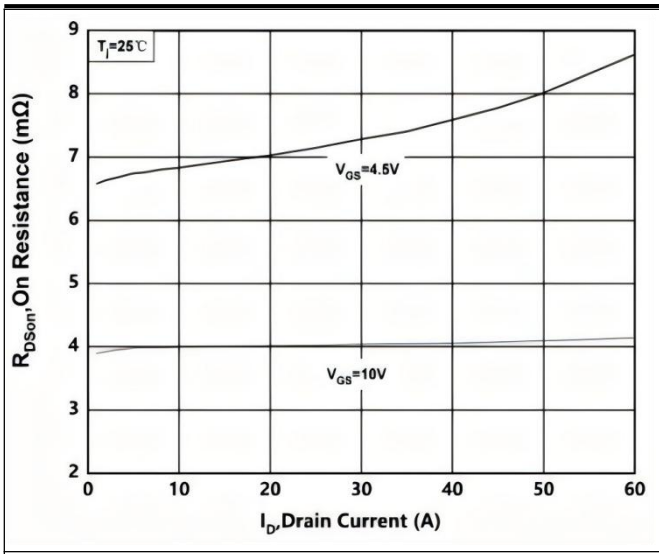


Fig 5: Typical Threshold Voltage vs Junction Temperature

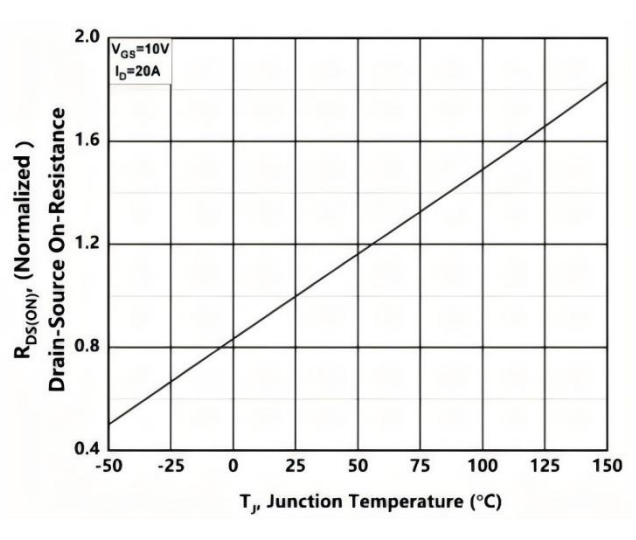


Fig 6: Typical Breakdown Voltage vs Junction Temperature

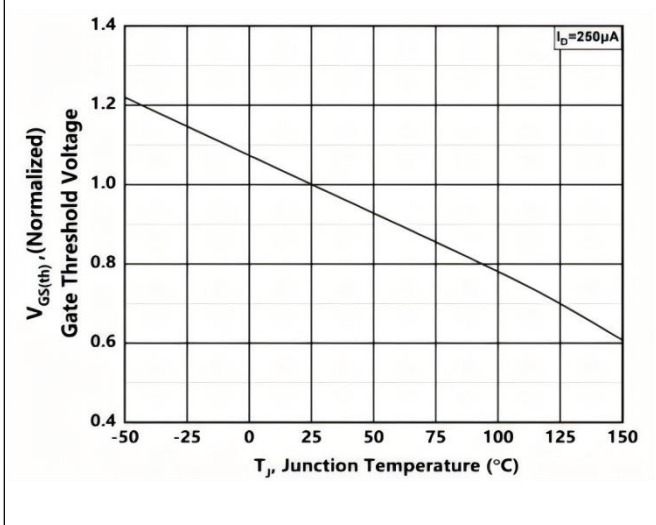


Fig 7: Typical Capacitance vs Drain to Source Voltage

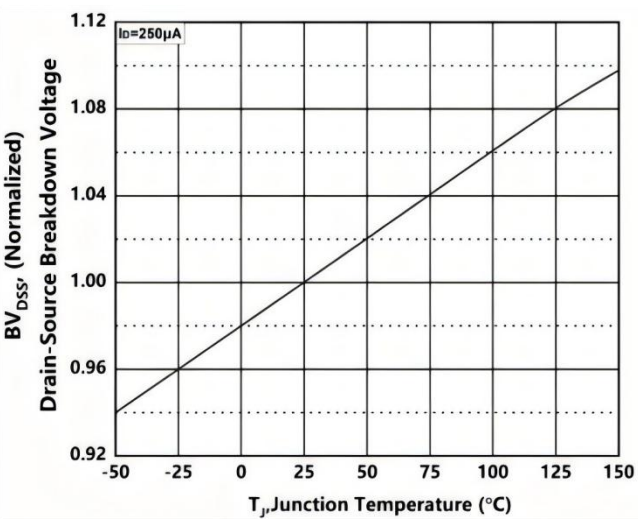


Fig 8: Typical Gate Charge vs Gate to Source Voltage

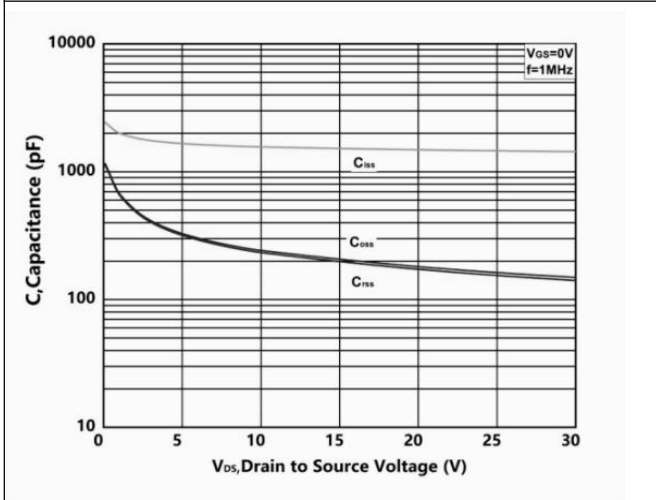


Fig 9: Typical Body Diode Characteristics

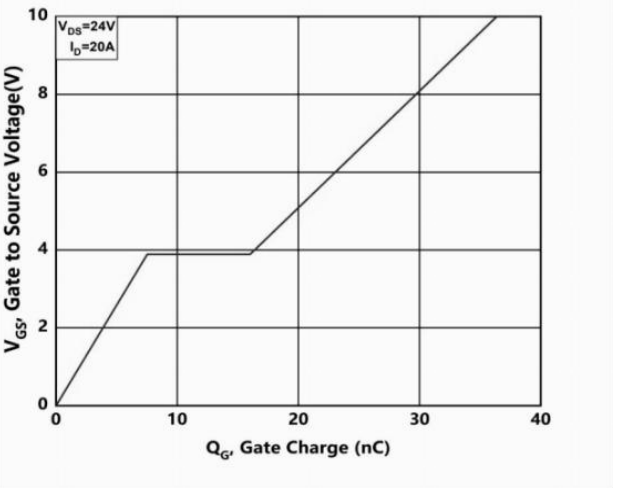


Fig 10: Maximum power Dissipation Derating vs Case Temperature

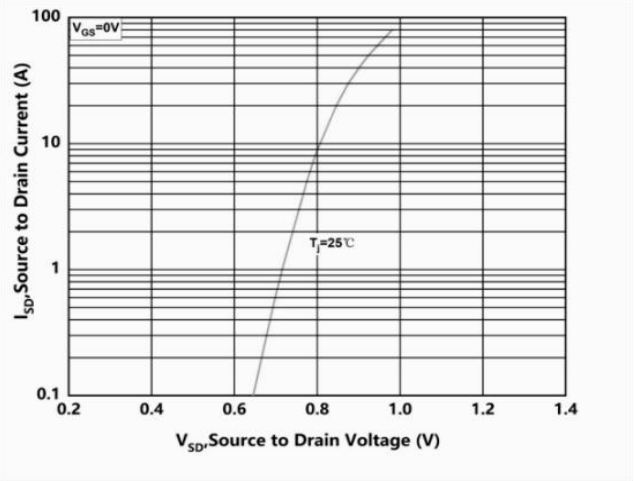


Fig 11: Continuous Drain Current Derating vs Case Temperature

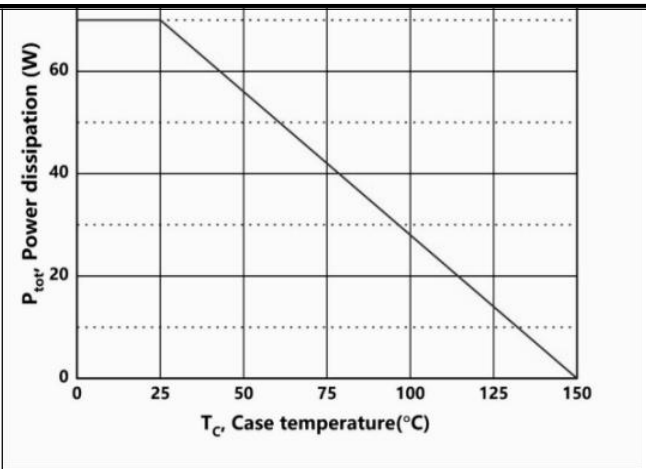
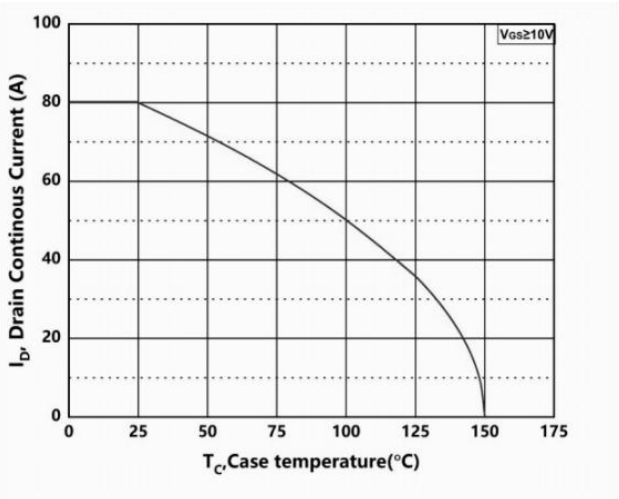


Fig 12: Safe Operating Area



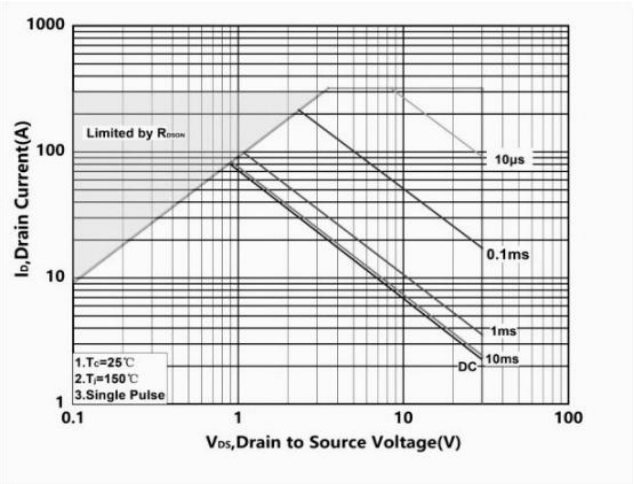
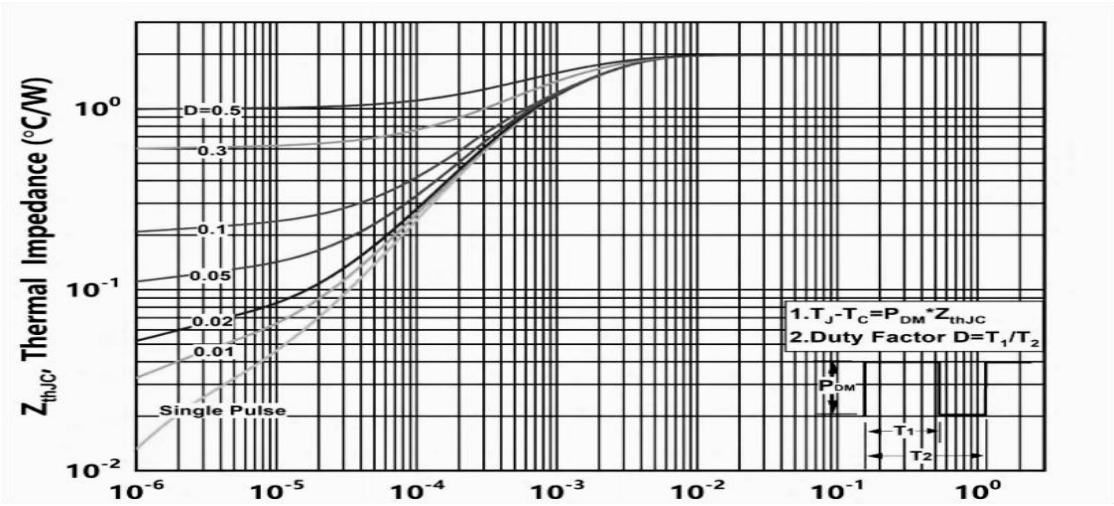


Fig 13: Transient Thermal Impedance (Junction - Case)



TEST CIRCUITS AND WAVEFORMS

Fig A:Peak Diode Recovery dv/dt Test Circuit & Waveforms

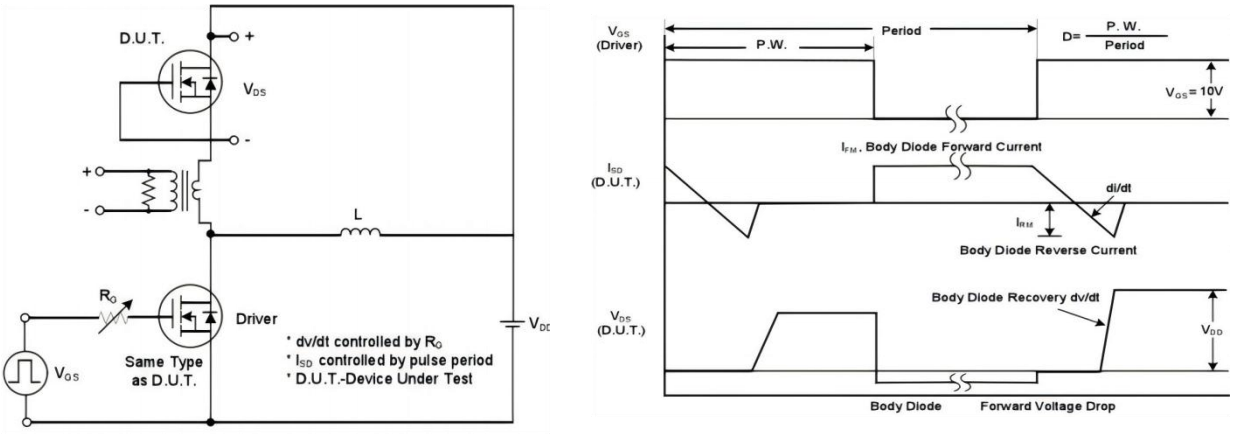


Fig B: Switching Test Circuit & Waveforms

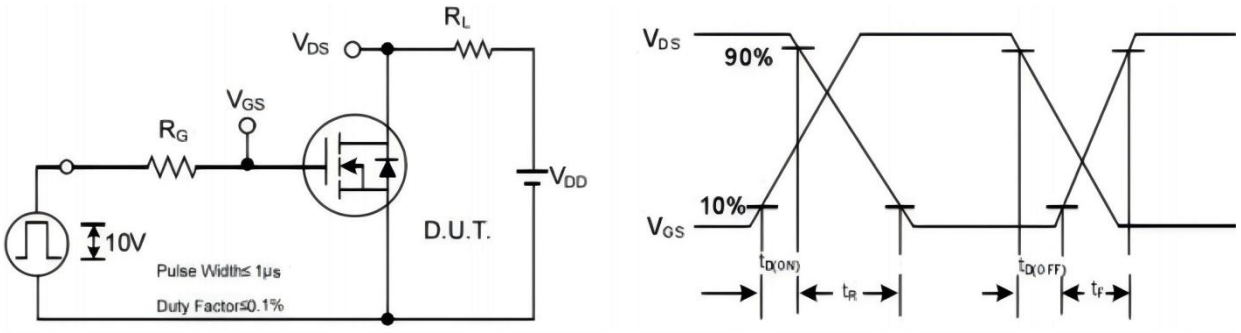


Fig C: Unclamped Inductive Switching Test Circuit & Waveforms

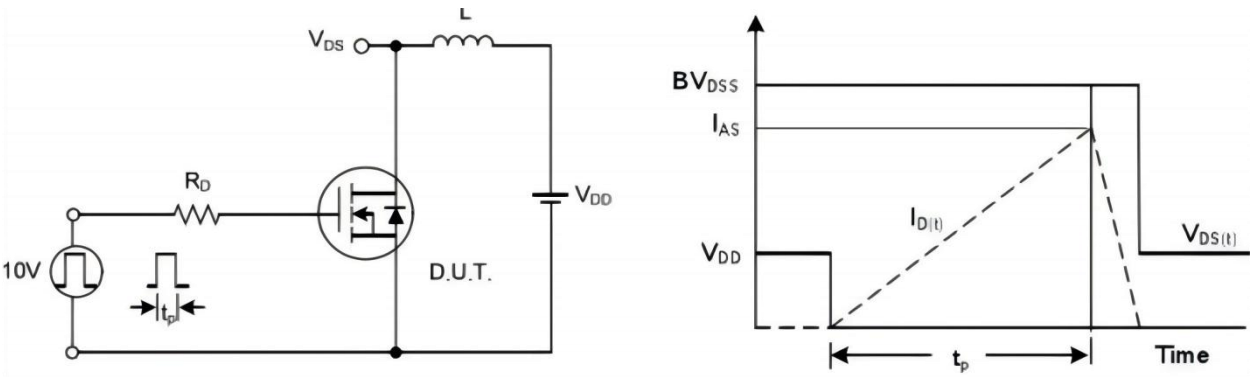
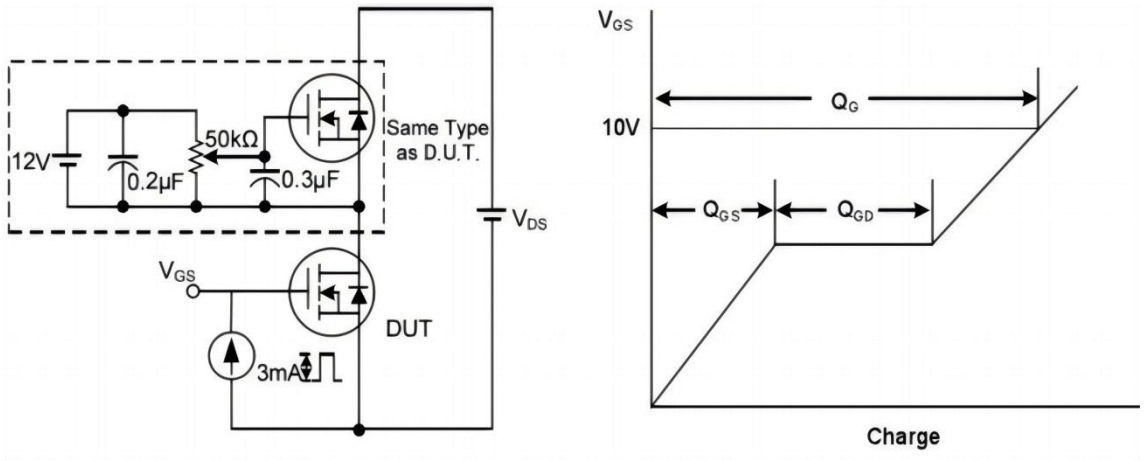
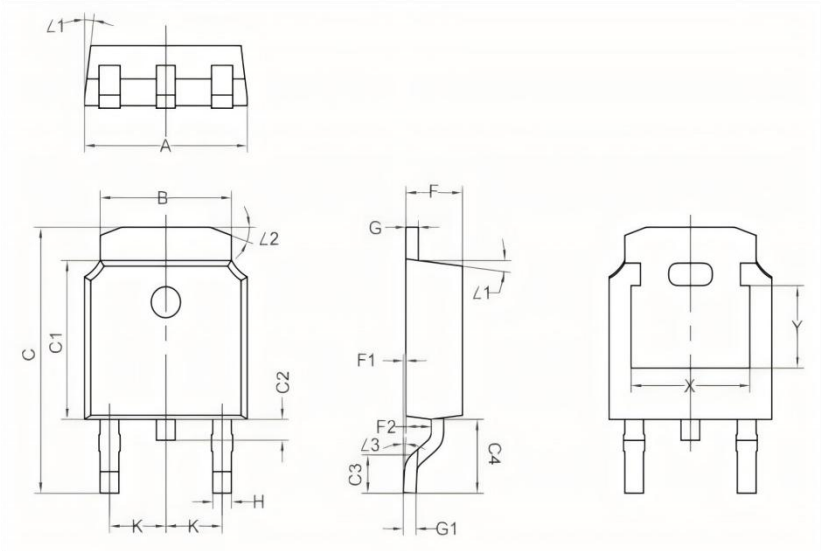


Fig D: Gate ChargeTest Circuit & Waveforms



PACKAGE OUTLINES (unit:mm)

TO-252



DIMENSIONS(unit:mm)		
Symbol	MIN	MAX
A	6.500	6.700
B	5.230	5.430
C	10.000	10.400
C1	6.000	6.200
C2	0.600	0.900
F	2.200	2.400
F1	0	0.100
F2	0.930	1.130
G	0.460	0.560
∠1	6°	8°
H	0.710	0.810
K	2.250	2.350
∠2	15°	20°
C3	1.350	1.650
G1	0.460	0.560
∠3	0°	5°
C4	2.800REF	
X	4.650	4.850
Y	3.000	3.200

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