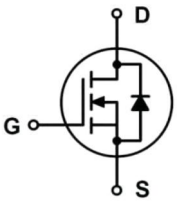
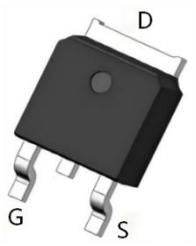
N-Channel Super Junction MOSFET

Parameter	Value	Unit
V_{DS}	800	V
$R_{DS(max)}$	400	mΩ
I_D	13	A





TO-252

Features

- Multi-layer Epitaxial Chip Technology
- Low On-Resistance
- Very low FOM RDS(on)×Qg
- Easy to use/drive

Applications

- Adapter
- PFC Power Supply Stages
- Switching Applications

Absolute Maximum Ratings (T_C=25℃,unless otherwise noted)

Symbol	Parameter		Value	Unit	Note
VDSS	Drain to Source Voltage		800	V	
VGSS	Gate to Source Voltage		±30	V	
ID	Drain Current (continuous)	VGS=10V, TC = 25℃	13	A	Fig 1
		VGS=10V, TC = 100℃	7.8		
IDM	Drain Current	Pulsed (Note1)	39	A	
EAS	Single Pulsed Avalanche Energy (Note2)		125	mJ	
IAR	Avalanche Current (Note2)		1.8	A	
dv/dt	MOSFET dv/dt		50	V/ns	
	Peak Diode Recovery dv/dt (Note3)		15		
PD	Power Dissipation	(TC = 25℃)	105	W	
EAS	Repetitive Avalanche Energy		125	mJ	
TJ, TSTG	Operating and Storage Temperature Range		-55 to 150	℃	

Thermal Data

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.2	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62	
T_{sold}	Soldering temperature, wave soldering only allowed at leads	260	℃

Electrical Characteristics(T_J=25℃,unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Note
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	800	-	-	V	Fig 8
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V	-	-	1	μA	
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±30 V	-	-	± 100	nA	
On Characteristics							
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 uA	2.5	3.5	4.5	V	Fig 2
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 6.5A , T_J = 25℃	-	350	400	mΩ	Fig 3
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} =0 V f = 1 MHz	-	1134.6	-	pF	Fig 4
C_{oss}	Output Capacitance		-	31.1	-	pF	
C_{rss}	Reverse transfer capacitance		-	0.29	-	pF	
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS}= 640V I_D =6 A, V_{GS} =10 V	-	27	-	nC	Fig 5
Q_{gs}	Gate to Source Charge		-	6.18	-	nC	
Q_{gd}	Gate to Drain “Miller” Charge		-	11.7	-	nC	
R_G	Gate Resistance	f = 1 MHz, Open Drain	-	11.7	-	Ω	
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 400V I_D = 5 A, R_G = 25Ω	-	45.1	-	ns	
t_r	Turn-On Rise Time		-	32.3	-	ns	
$t_{d(off)}$	Turn-Off Delay Time		-	147.2	-	ns	
t_f	Turn-Off Fall Time		-	39.6	-	ns	
Source-Drain Diode Characteristics							
V_{SD}	Diode Forward Voltage	T_J = 25ºC, I_{SD} = 6.5A, V_{GS} = 0V	-	0.9	1.2	V	
I_{mm}	Peak Reverse Recovery Current	V_R = 400V , I_F=30A diF/dt = 100A/μs	-	22.6	-	A	
t_{rr}	Reverse Recovery Time		-	350.6	-	ns	
Q_{rr}	Reverse Recovery Charge		-	4.94	-	μC	

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L=10mH, RG = 25 Ω, starting TJ = 25℃ .
3. Identical low side and high side switch with identical RG

Typical Characteristics

Figure 1. Output Characteristics

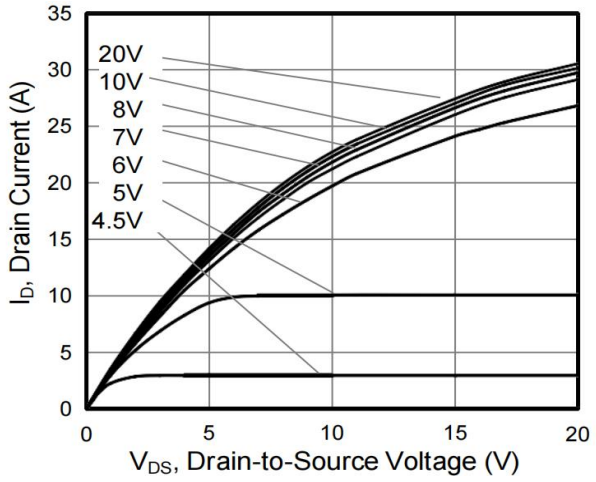


Figure 2. Transfer Characteristics

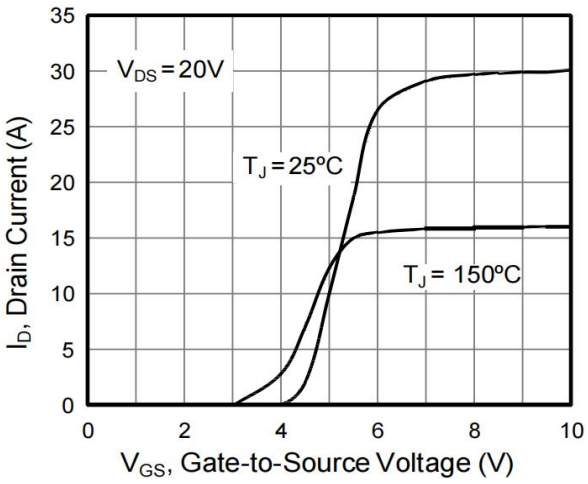


Figure 3. On-Resistance vs. Drain Current

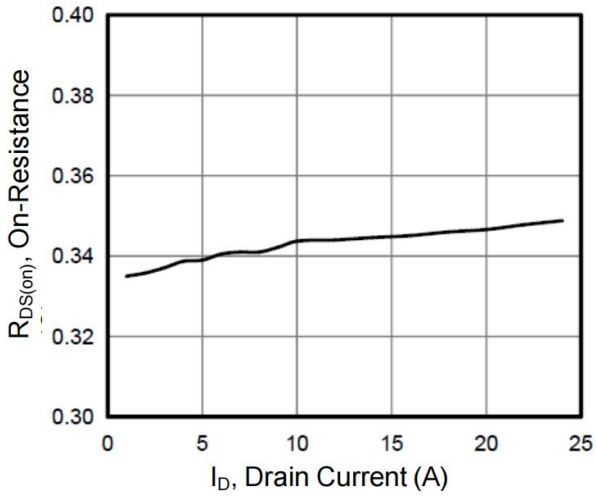


Figure 4. Capacitance

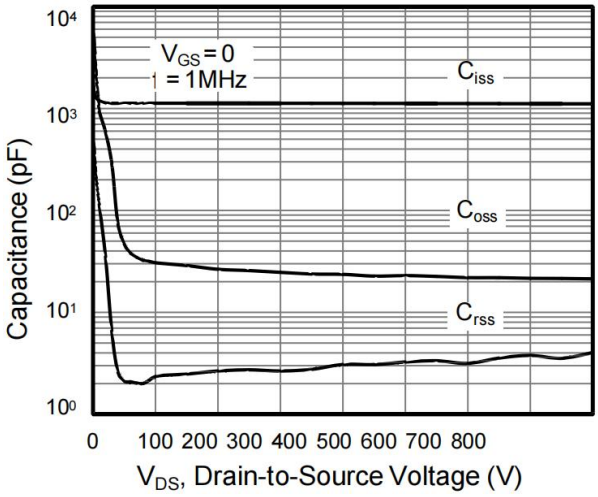


Figure 5. Gate Charge

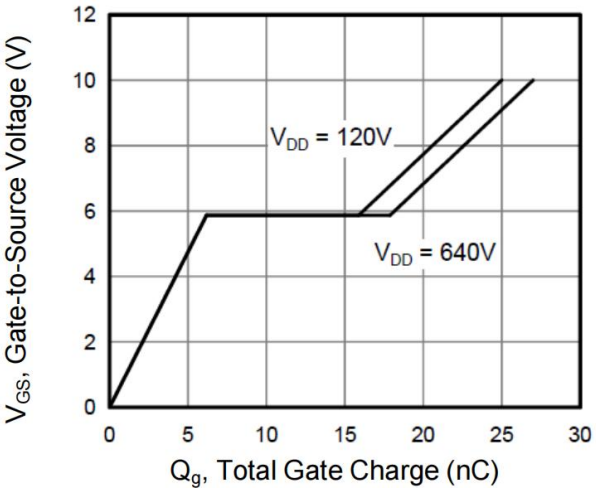


Figure 6. Body Diode Forward Voltage

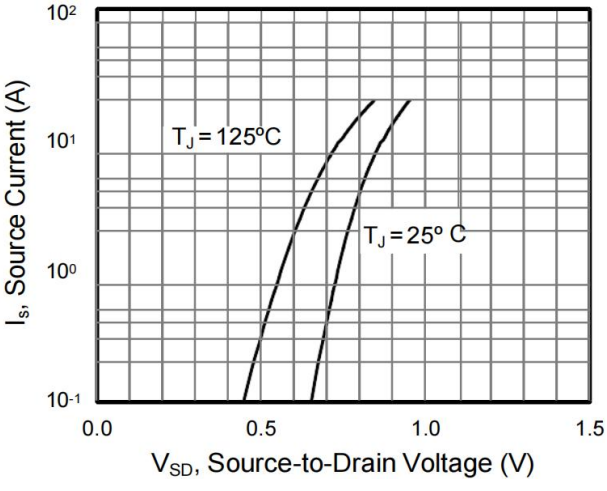


Figure 7. On.Resistance vs.Temperature

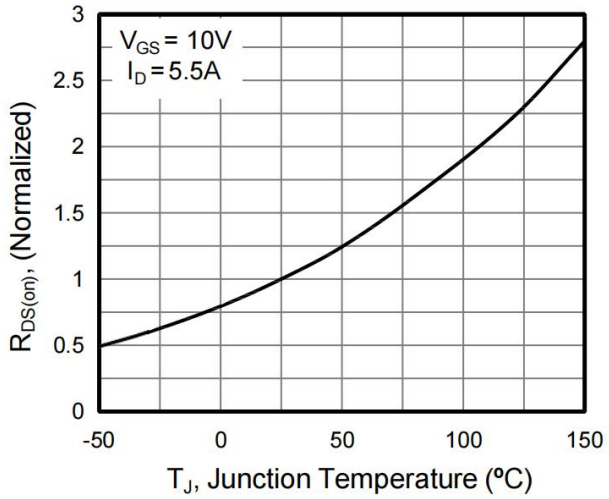


Figure 8. Breakdown Voltage vs.Junction Temperature

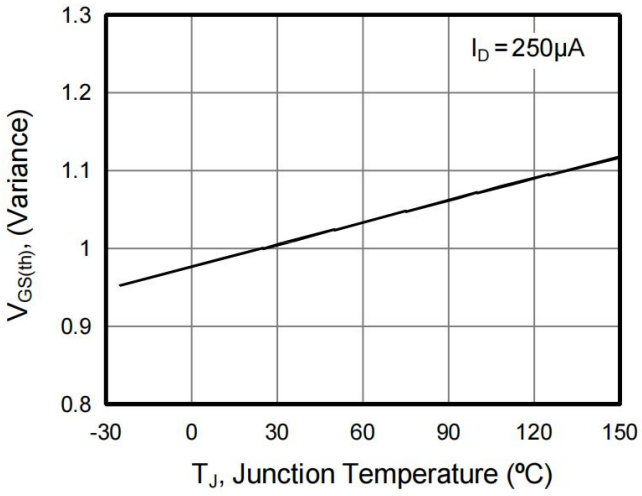


Figure 9. Transient Thermal Impedance

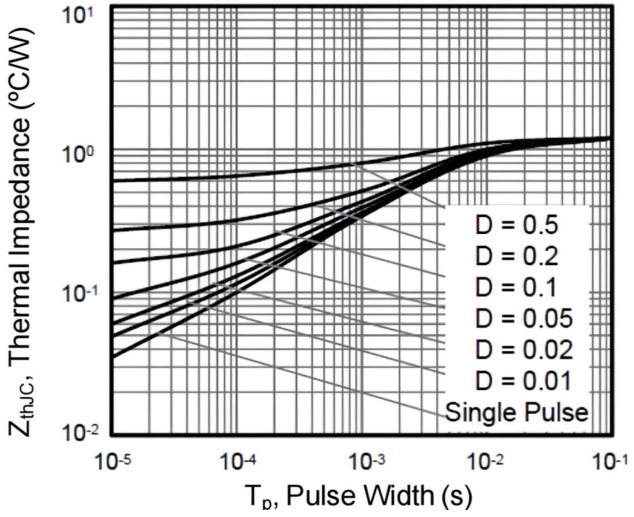


Figure 10. Safe Operation Area

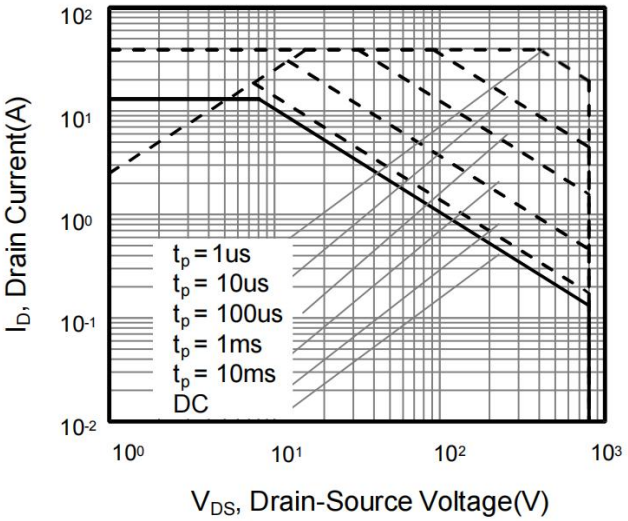
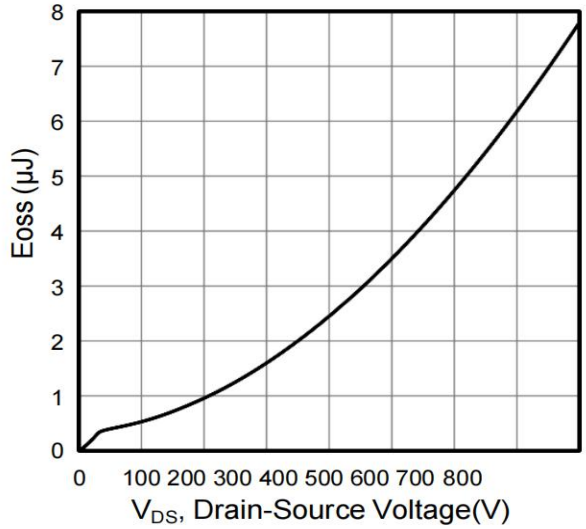


Figure 11. Typ. Coss Stored Energy



Test Circuits

Figure 12 ： Gate Charge Test Circuit and Waveform

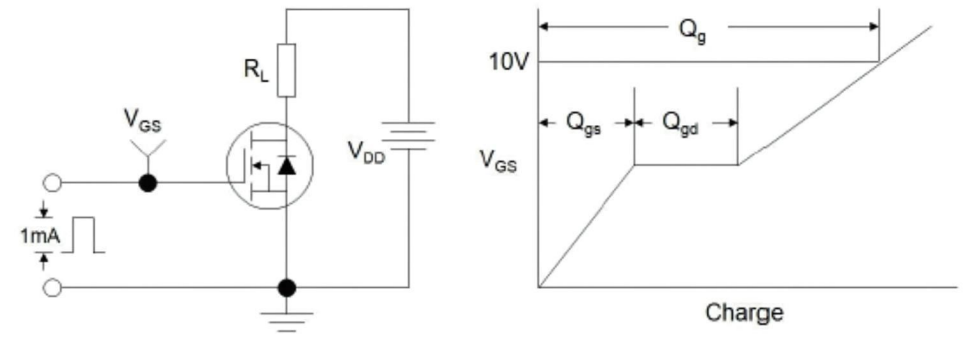


Figure 13 ： Resistive Switching Test Circuit and Waveform

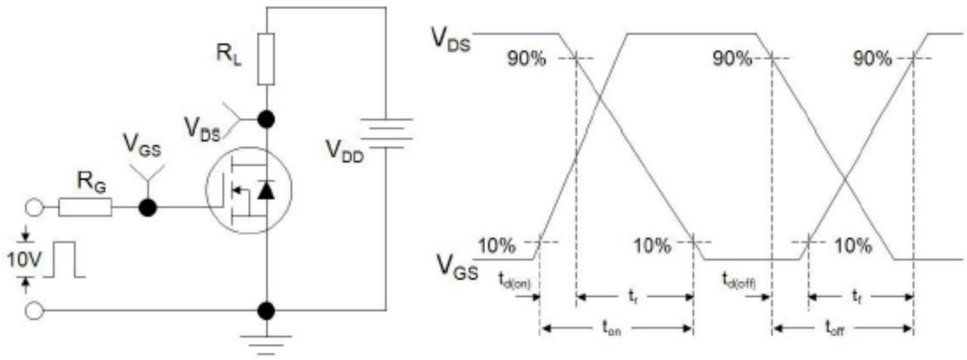
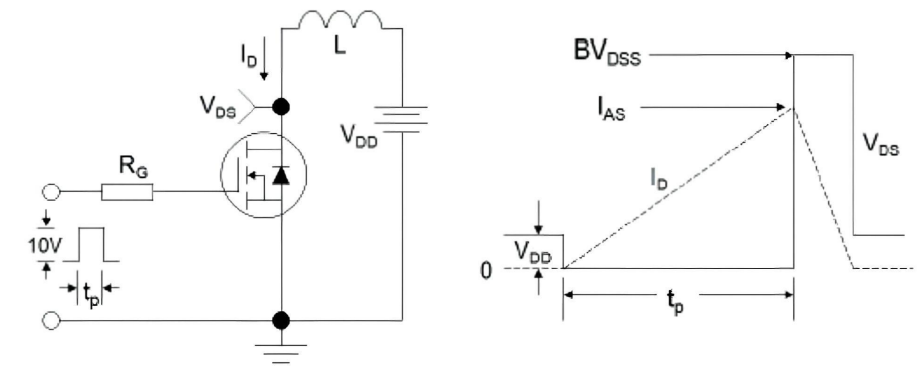
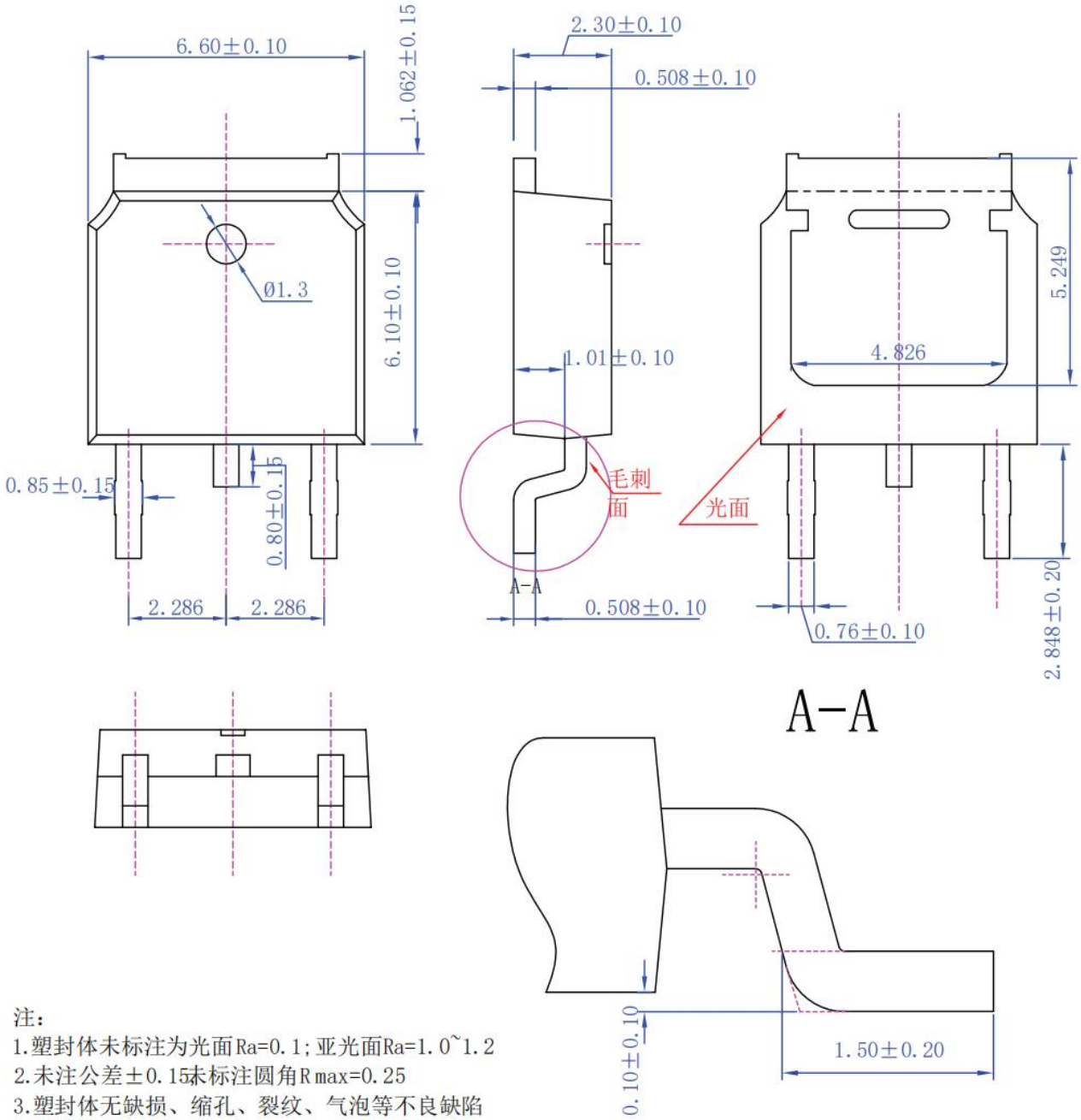


Figure 14 ： Unclamped Inductive Switching Test Circuit and Waveform



Package Outline(Unit :mm) TO-252



注：
1.塑封体未标注为光面Ra=0.1；亚光面Ra=1.0~1.2
2.未注公差±0.15未标注圆角R max=0.25
3.塑封体无缺损、缩孔、裂纹、气泡等不良缺陷
4.标注单位mm
5.顶针孔不允许凸出塑封体表面

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