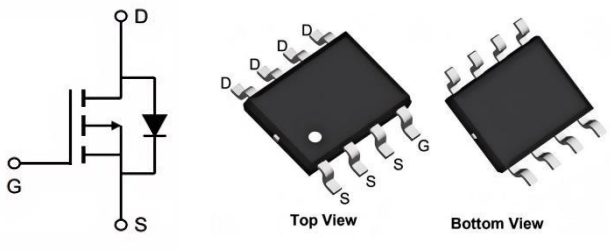
P-Channel Enhancement Mode MOSFET

Parameter	Value	Unit
V_{DS}	-30	V
$R_{DS(on)}$	10	mΩ
I_D	-12.5	A



SOP-8

Features

- Advanced trench cell design
- Low Thermal Resistance
- Low Gate Charge

Applications

- Motor/Body Load Control
- Load Switch
- DC-DC converters and Off-line UPS

Absolute Maximum Ratings (T_A=25℃,unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	-12.5	A
	T_C=70℃		-8.5	
Pulsed Drain Current [1]		I_{DM}	-44	A
Single Pulse Avalanche Energy [2]		E_{AS}	53	mJ
Total Power Dissipation	T_C=25℃	P_D	4.8	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance from Junction to Ambient [1]	$R_{\theta JA}$	---	75	℃/W
Thermal Resistance Junction-Ambient [1](t≤10s)		---	40	℃/W
Thermal Resistance Junction-Case1	$R_{\theta JC}$	---	24	℃/W

Electrical Characteristics(T_J=25℃,unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V , I_D=-250uA	-30	-	-	V
BVDSS Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	Reference to 25℃,I_D=-1mA	-	-	-	V/℃
Static Drain-Source On-Resistance2	$R_{DS(ON)}$	V_{GS}=-10V , I_D=-1A	-	10	13	mΩ
		V_{GS}=-4.5V , I_D=-1A	-	15	20	
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} , I_D=-250uA	-1.0	-	-2.5	V
VGS(th) Temperature Coefficient	$\triangle V_{GS(th)}$		-	-	-	mV/℃
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-30V , V_{GS}=0V , T_J=25℃	-	-	-1	uA
		V_{DS}=-30V , V_{GS}=0V , T_J=55℃	-	-	-5	
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ±20V , V_{DS}=0V	-	-	±100	nA
Gate Resistance	R_g	V_{DS}=0V , V_{GS}=0V , f=1MHz	-	-	-	Ω
Total Gate Charge (-4.5V)	Q_g	V_{DS}=-15V , V_{GS}=-4.5V , I_D=-5A	-	26	-	nC
Gate-Source Charge	Q_{gs}		-	1.2	-	
Gate-Drain Charge	Q_{gd}		-	2.4	-	
Turn-On Delay Time	$T_{d(on)}$	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3Ω , I_D=-5A	-	11	-	ns
Rise Time	T_r		-	15	-	
Turn-Off Delay Time	$T_{d(off)}$		-	52	-	
Fall Time	T_f		-	24	-	
Input Capacitance	C_{iss}	V_{DS}=-15V , V_{GS}=0V , f=1MHz	-	1810	-	pF
Output Capacitance	C_{oss}		-	241	-	
Reverse Transfer Capacitance	C_{rss}		-	213	-	

Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Continuous Source Current [1,5]	I_S	V_G=V_D=0V , Force Current	-	-	-12.5	A
Pulsed Source Current [2,5]	I_{SM}		-	-	-44	A
Diode Forward Voltage [2]	V_{SD}	V_{GS}=0V , I_S=-1A , T_J=25℃	-	-	-1.2	V

Note :
1.The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
3. The EAS data shows Max. rating . The test condition is VDD=-25V,VGS=-10V,L=0.1mH,IAS=-38A
4. The power dissipation is limited by 150℃ junction temperature
5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

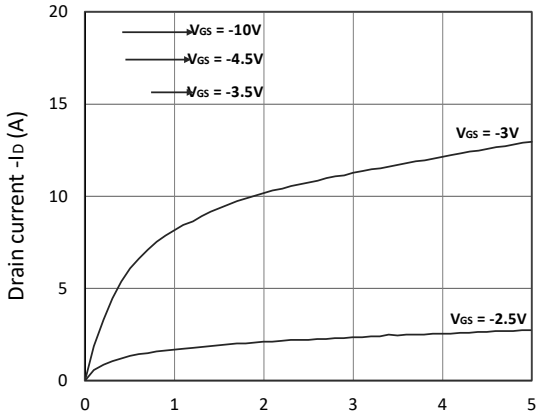


Figure 1. Output Characteristics

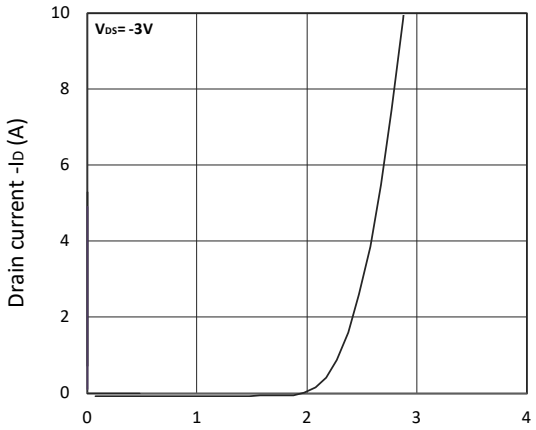


Figure 2. Transfer Characteristics

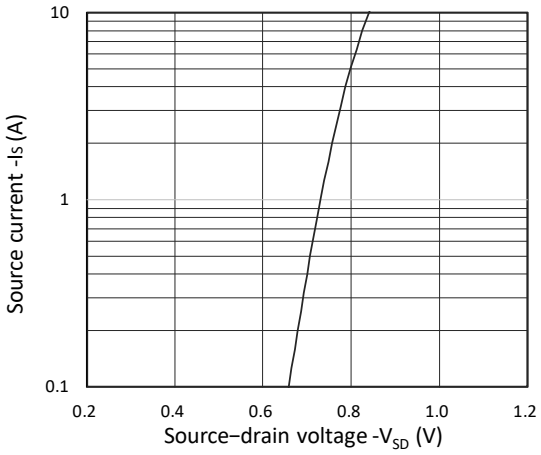


Figure 3. Forward Characteristics of Reverse

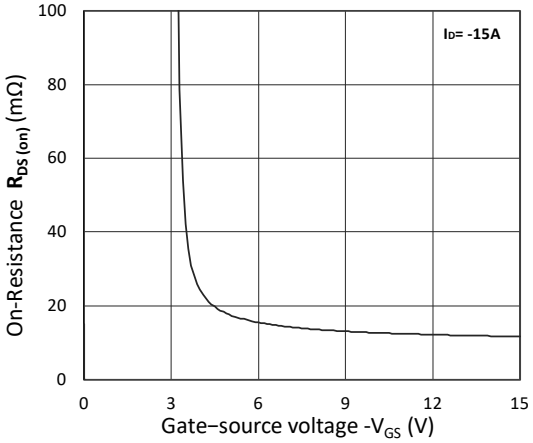


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

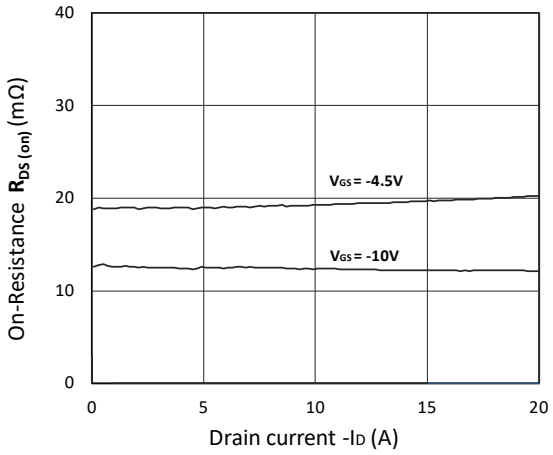


Figure 5. $R_{DS(ON)}$ vs. I_D

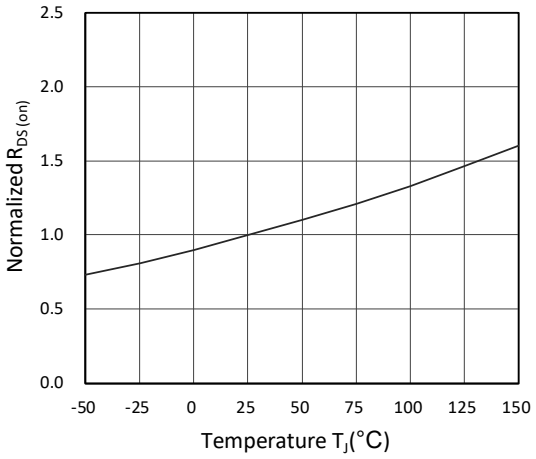


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

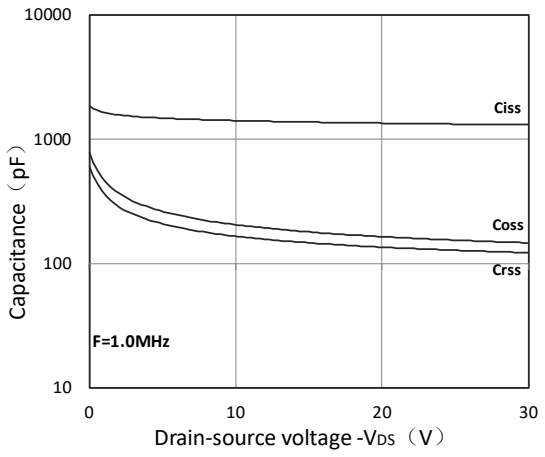


Figure 7. Capacitance Characteristics

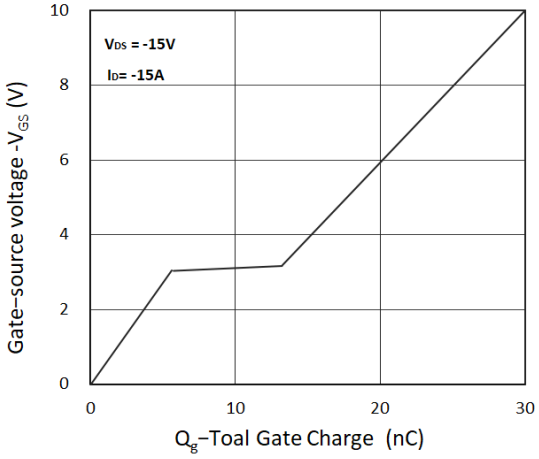


Figure 8. Gate Charge Characteristics

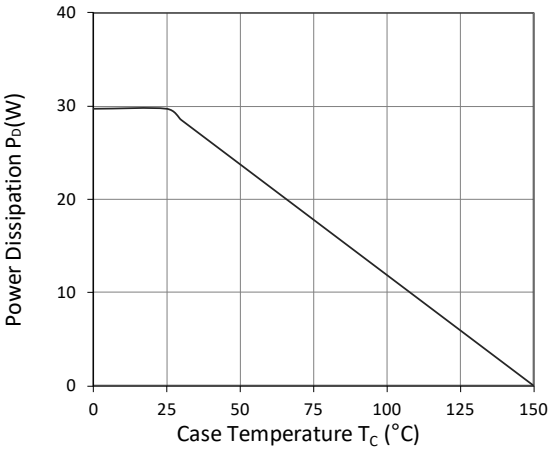


Figure 9. Power Dissipation

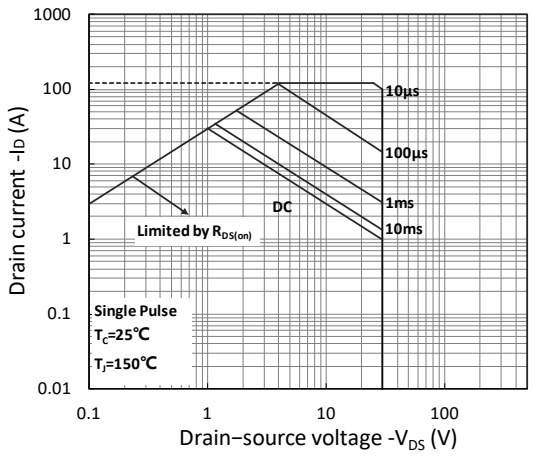


Figure10. Safe Operating Area

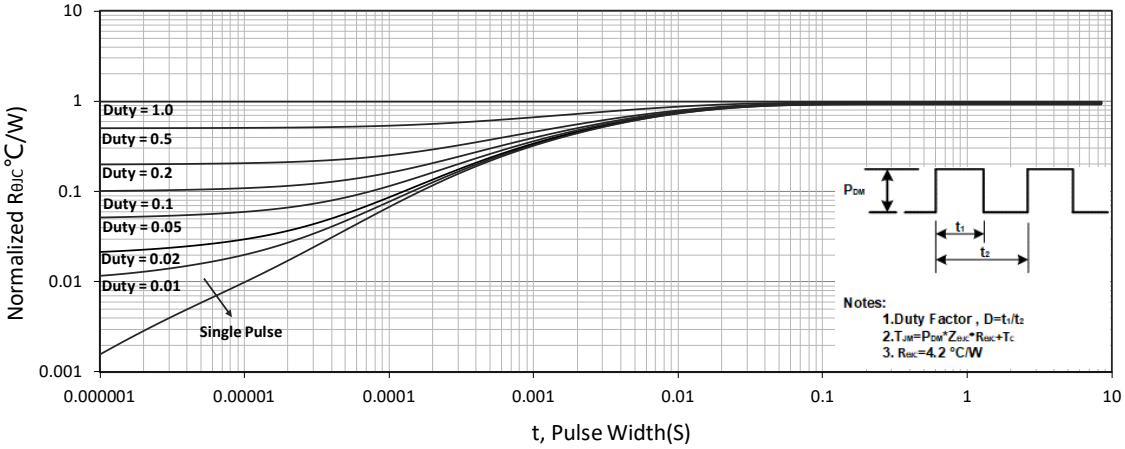
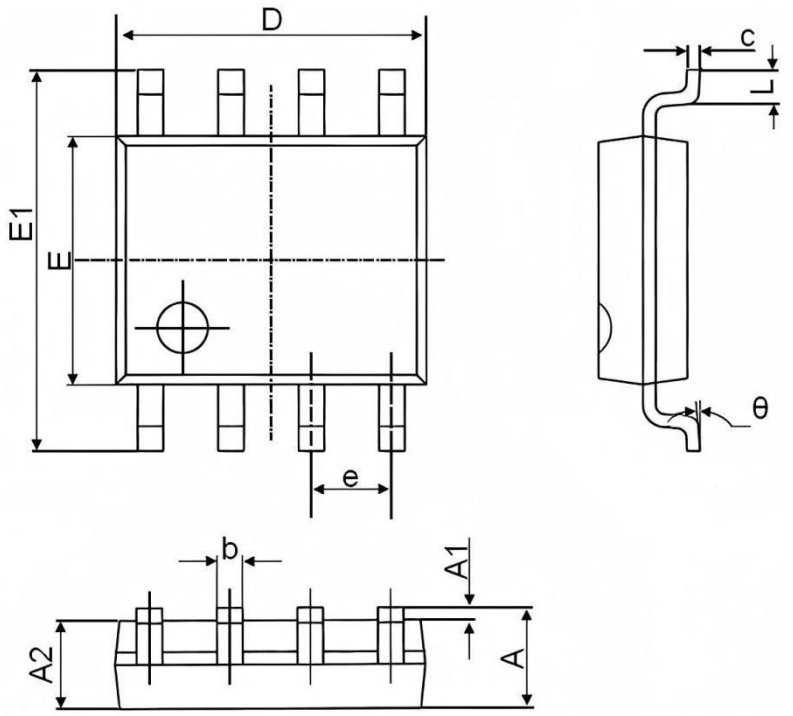


Figure 11. Normalized Maximum Transient Thermal Impedance

Package Outlines Dimensions (Units: mm)

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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